(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 350 057 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication of patent specification: **01.12.93**

(51) Int. Cl.5: **G11C 11/24**, G11C 7/00, G11C 11/412

(21) Application number: **89112468.7**

(22) Date of filing: **07.07.89**

(54) Semiconductor memory.

(30) Priority: **07.07.88 JP 169930/88**

(43) Date of publication of application:
10.01.90 Bulletin 90/02

(45) Publication of the grant of the patent:
01.12.93 Bulletin 93/48

(84) Designated Contracting States:
DE FR GB

(56) References cited:
EP-A- 0 031 238
EP-A- 0 157 051
US-A- 4 259 729

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EP 0 350 057 B1

According to the present invention, since the substrate of the MOS transistor of the MOS dynamic semiconductor memory cell is not connected to a fixed potential terminal, the substrate potential of the MOS transistor can be time-selectively switched and controlled. Therefore, the memory cell characteristics depending on the substrate potential can be controlled to avoid the Vth increase according to the bit line level, or can be switched and controlled to an enhancement type or a depletion type, as needed.

The semiconductor memory having the above-mentioned memory cell array can time-selectively switch and control the potential of the substrate so that the MOS transistor can avoid the Vth increase due to the back-gate bias effect according to the bit line level, or so that the MOS transistor becomes an enhancement type or a depletion type which can prevent a threshold voltage loss. Therefore, a memory cell selected in response to an address signal can be controlled to avoid the Vth increase or to be of the depletion type. Therefore, the threshold voltage loss of the semiconductor memory cell can be minimized or prevented. Even if the limit level of the logical amplitude of the bit lines is used as an enable voltage of the word line, data can be written up to the limit level of the logical amplitude of the bit lines of the semiconductor memory cell. Therefore, when the semiconductor memory cell is operated, a word line booster is simplified or not required, and the operation margin and reliability of the memory cell element can be improved.

The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawing, in which:

Fig. 1 is a sectional view of a conventional MOS dynamic memory cell;

Fig. 2 is an equivalent circuit of a conventional MOS dynamic memory cell shown in Fig. 1;

Fig. 3 is a typical relationship between a threshold voltage and a substrate potential of the enhancement type MOS transistor;

Fig. 4 is an equivalent circuit of a MOS dynamic memory cell used in a memory cell array of a C MOS dynamic RAM;

Fig. 5 is an example of a conceptional structure of the memory cell;

Fig. 6 is a relationship of between a threshold voltage and a substrate potential of the MOS transistor shown in Fig. 5;

Fig. 7 is a relationship between a potential of a word line and that of a substrate potential line of the MOS transistor shown in Fig. 5;

Figs. 8 and 9 are sectional views of different embodiment; and

Fig. 10 is an equivalent circuit of another embodiment shown in Fig. 9.

An embodiment of the present invention will be described hereinafter in detail with reference to the accompanying drawings.

Fig. 4 shows an equivalent circuit of a MOS dynamic memory cell MC used in a memory cell array of a CMOS dynamic RAM. In this memory cell MC, one terminal of a current path of one MOS transistor (e.g., an n-channel type) T is connected to one capacitor element C, the other terminal thereof is connected to a bit line BL, and a gate electrode G is connected to a word line WL. Note that a back gate of the MOS transistor T is connected to a substrate potential line 10, and the substrate potential line 10 is connected to a potential switching device Vbb for time-selectively switching the potential of the substrate potential line 10.

Fig. 5 shows an example of a conceptional structure of the memory cell MC. Reference numeral 1 denotes a semiconductor substrate; 2, a p-type substrate layer (well region) formed in a memory cell formation region of the semiconductor substrate 1; 3, a gate oxide film formed on the p-type substrate layer 2; 4, a capacitor insulating film formed on the p-type substrate layer 2; 5, an element isolation region; 6 and 7, drain region and source region n-type impurity layers formed in the p-type substrate layer 2; 8, an n-type impurity layer for electric charge storage formed in the p-type substrate layer 2; 9, a capacitor electrode of polysilicon formed on the capacitor insulating film 4; and G, a gate electrode of polysilicon formed on the gate oxide film 3. The p-type substrate layer 2 is connected to the substrate potential line 10 disposed in the same direction as that of the word line WL when the memory cells are arranged in a matrix form. The potential of the substrate potential line 10 is not fixed but can be time-selectively switched by the potential switching device Vbb in the semiconductor memory. This switching device Vbb is controlled in response to an address signal associated with, e.g., word line selection.

Since the substrate layer 2 of the MOS transistor is not connected to a fixed potential terminal, the above-mentioned memory cell can time-selectively switch and control the substrate potential of the MOS transistor. Therefore, the electric characteristic of the memory cell can be switched and controlled by a substrate bias effect either to avoid the Vth increase according to the bit line level or to be of an enhancement type or a depletion type which can prevent a threshold voltage loss. More specifically, the relationship between a threshold voltage Vth of the MOS transistor and its substrate potential Vbb is shown in Fig. 6. When a substrate potential Vbboff is applied to the substrate layer 2,

transistor at every predetermined period of time so that said MOS transistor becomes an enhancement type or a depletion type which can prevent a threshold voltage loss.

3. A memory according to claim 1, characterized in that said memory cell comprises a well region of a second conductivity type formed in a semiconductor substrate of a first conductivity type, said MOS transistor being of a first channel type and formed on a surface of said well region, a third impurity layer for electric charge storage of the first conductivity type formed on the surface of said well region to be in contact with a first or second impurity layer of said MOS transistor, and a capacitor electrode disposed on said third impurity layer through a capacitor insulating film.

4. A memory according to claim 1, characterized in that said memory cell comprises a semiconductor region (53) of a second conductivity type formed in a insulating layer (52) which is formed on a semiconductor substrate (51), said MOS transistor (T) being of a first channel type and formed on a surface of said semiconductor region (53), a third impurity layer for storing electrical charge, said third impurity layer being of the first conductivity type and formed on a surface of said insulating layer (52) by stretching either a first or second impurity layer (54, 55) of said MOS transistor into said insulating layer (52), and a capacitor electrode (58) formed on a capacitor insulating film (57) which is formed on said third impurity layer.

5. A memory according to claim 1, characterized in that potential switching device (Vbb) is controlled by timing pulses for selecting said word line (WL).

6. A memory according to claim, 2 characterized in that said potential switching device (Vbb) is controlled by timing pulses for selecting said word line (WL).

7. A memory according to claim 3, characterized in that said potential switching device (Vbb) is controlled by timing pulses for selecting said word line (WL).

8. A memory according to claim 4, characterized in that said potential switching device (Vbb) is controlled by timing pulses for selecting said word line (WL).

Patentansprüche

1. Halbleiterspeicher, umfassend:
eine Bitleitung und eine Wortleitung;
eine Speicherzelle mit einem Kondensatorelement und einem MOS-Transistor, dessen einer Strompfad mit dem Kondensator verbunden ist, dessen anderer Strompfad mit der Bitleitung verbunden ist und dessen Gate-Elektrode mit der Wortleitung verbunden ist; und
eine Substratpotentialleitung, die mit einem Rück-Gate des MOS-Transistors verbunden ist;
gekennzeichnet durch
eine Potential-Schalteinrichtung, die mit der Substratpotentialleitung verbunden ist, um ein Potential des Rück-Gates des MOS-Transistors zu steuern.

2. Speicher nach Anspruch 1,
dadurch **gekennzeichnet**, daß die Potential-Schalteinrichtung das Potential des Rück-Gates des MOS-Transistors zu jeder vorgegebenen Zeitperiode so steuert, daß der MOS-Transistor zu einem Anreicherungs-Typ oder einem Verarmungs-Typ wird, was einen Schwellspannungsverlust verhindern kann.

3. Speicher nach Anspruch 1,
dadurch **gekennzeichnet**, daß die Speicherzelle einen in einem Halbleitersubstrat eines ersten Leitfähigkeitstyps gebildeten Wannenbereich eines zweiten Leitfähigkeitstyps umfaßt, wobei der MOS-Transistor von einem ersten Kanaltyp ist und auf einer Oberfläche des Wannenbereichs gebildet ist, eine auf der Oberfläche des Wannenbereichs gebildete dritte Verunreinigungsschicht des ersten Leitfähigkeitstyps zur Speicherung von elektrischen Ladungen, um mit einer ersten und zweiten Verunreinigungsschicht des MOS-Transistors in Kontakt zu stehen und eine Kondensatorelektrode, die sich über einen Kondensator-Isolationsfilm auf der dritten Verunreinigungsschicht befindet.

4. Speicher nach Anspruch 1,
dadurch **gekennzeichnet**, daß die Speicherzelle einen Halbleiterbereich (53) eines zweiten Leitfähigkeitstyps umfaßt, der in einer Isolationsschicht (52) gebildet ist, die auf einem Halbleitersubstrat (51) gebildet ist, wobei der MOS-Transistor (T) von einem ersten Kanal-Typ ist und auf einer Oberfläche des Halbleiterbereichs (53) gebildet ist, eine dritte Verunreinigungsschicht zum Speichern von elektrischen Ladungen, wobei die dritte Verunreinigungsschicht von dem ersten Leitfähigkeitstyp ist und auf einer Oberfläche der Isolations-

sions de cadencement pour sélectionner ladite ligne de mot (WL).

8. Mémoire selon la revendication 4, caractérisée en ce que ledit dispositif de commutation de potentiel (Vbb) est commandé par les impulsions de cadencement pour sélectionner ladite ligne de mot (WL).

FIG. 5

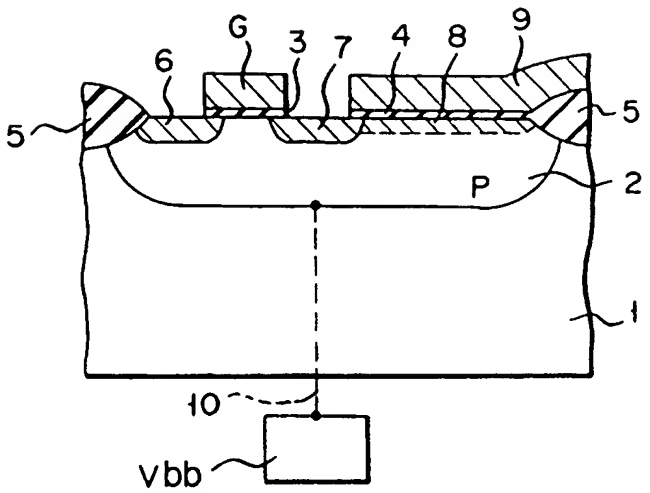

FIG. 6

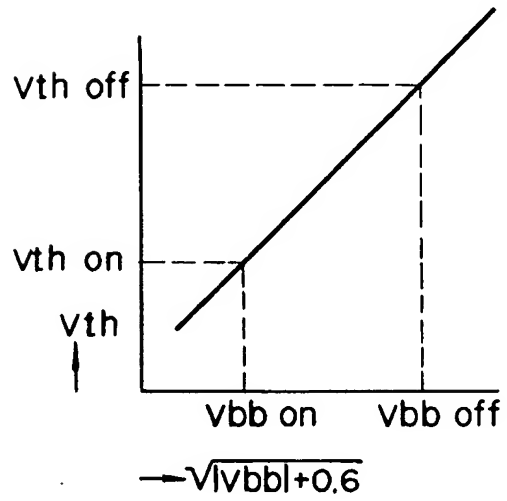

FIG. 7